REMARKS

Claims 4-20 are pending in this application of which claims 4 and 5 are independent. Claims 5-13 and 15 stand allowed. Claims 4 and 14 have been rejected. Claims 16-20 have been added. Care has been taken to avoid the introduction of new matter.

Following the Request for Reconsideration filed on April 7, 2004, the Examiner withdrew the obviousness rejection of claims 4 and 14. (See Office Action, section 3). However, the Examiner now rejects claims 4 and 14 citing the same references on new grounds. Specifically, claims 4 and 14 have been rejected under 35 U.S.C. §103(a) as being unpatentable over the so-called admitted prior art ("APA") (Fig. 8) in view of Kobayashi. This rejection is respectfully traversed.

The Examiner maintains the same position with regards to the so-called APA, that Fig. 8 of the present application illustrates "a clock generating circuit," "a plurality of first latch circuits," and a "plurality of second latch circuits," as claim 4 recites. However, the Examiner acknowledges, with which Applicant agrees, that the so-called APA does not disclose a control circuit for outputting a control signal to the second latch circuits according to a change in the input data signal after a prescribed period of time.

Referring to Fig. 6 of Kobayashi, the Examiner contends that inverters 9a, 9c and 9h and transfer gates 10a and 10b collectively form a pulse generating circuit for generating a pulse signal (at node N2, Fig. 6) according to a change in the input data signal, as claim 4 recites. The Examiner further contends that the series of inverters 9b, 9d, 9e and 9f for receiving a signal at N2 and outputting the data latch signal DL collectively form a delay circuit, as claim 4 recites.

Claim 4 has been amended to recite that the delay circuit enters a meta-stable state for at least part of, but not more than, the prescribed period of time to cause the delay. Exemplary support for this amendment can be found in the second embodiment described in the application.

The so-called APA and Kobayashi fail to disclose delay circuit (i.e., inverters 9b, 9d, 9e and 9f of Kobayashi), or any circuitry for that matter, entering a meta-stable state to cause at least part of, but not more than, the prescribed delay, as amended claim 4 recites. Claim 4 therefore is patentably distinguishable and allowable.

Dependent claims 14 and 16-20 are patentable at least based on dependency from allowable claim 4. New claims 16-20 recite components of the delay circuit, pulse generating circuit and control circuit, and further recites a level determination circuit. These elements are similarly recited dependent claims 6-13, which have been allowed.

All outstanding issues have been addressed by amending claim 4 to clearly distinguish over the combination of the so-called APA and Kobayashi. Withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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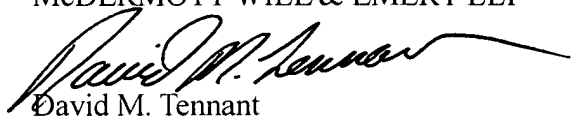

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